MT6765+MT6357 Co-Clock Design Notice

Revision History

Version	Date	Description	Author
V0.1	2017.10.19	Initial release (reference MT6739+MT6357)	Norris Lee / Steve Liu

Contents

- Crystal Placement and Layout Rule(Thermal consideration)
- AUXADC layout Rule
- XO Layout Rule for Clock Quality
- Clock Buffer Setting

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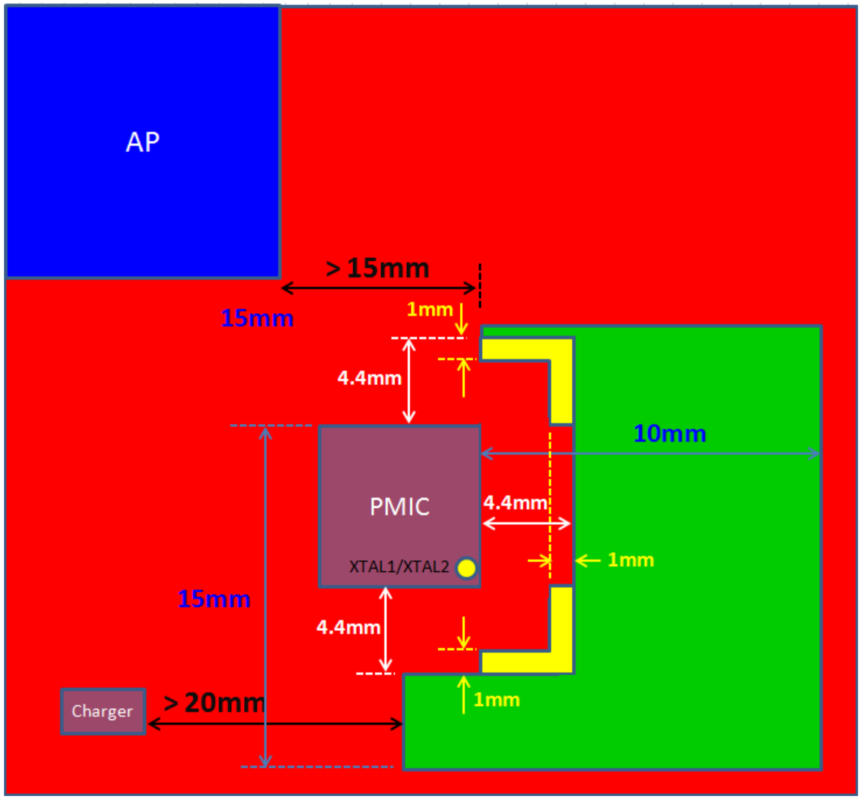
Crystal Placement and Layout Rule (Thermal Consideration)

Placement and Layout Rule

- TMS Placement Check Region for Thermal Consideration
  - Green Region : Recommended for TMS placement
  - Yellow Region : Marginal region for TMS placement. MTK's SW algorithm for cover boundary case.
  - Red Region : Risk region. RF performance might be degraded. It's sensitivity degraded by user scenarios.
- Others Consideration
  - AP should be far to MT6357/TMS **15mm** at least in horizontal distance.
  - **TIM** is recommended thermal solution for MT6357 platform.



- Green : Recommend Region
- Yellow : Marginal Region
- Red : Risk Region

Placement and Layout Rule

- Design Concept
  - This document is for reducing ***thermal*** impact for crystal. Please reserve enough area for crystal routing and keep-out region. The clock stability is very important for RF performance.
- Placement
  1. Keep the crystal and PMIC DCXO area **> 10 mm** away from the heat sources (i.e., **RF and WiFi PAs**).
  2. Keep the crystal **> 10 mm away from 1A charger, and > 20mm from 2A charger**.
  3. Keep the crystal **> 4.4 mm away from** PMIC, and **> 15 mm** away from **AP.**
  4. **Keep-out at least the first two inner layers** of metal including all crystal circuits.
  5. **Keep-out** all crystal components **> 0.25 mm** away from the surrounding metal.
  6. Do not place the crystal and PMIC DCXO area directly under the heat sources that on the opposite side (i.e., CPU, RF and WiFi PAs).
  7. Place the crystal inside the shielding case, and keep > 1 mm away from the PCB edge, and > 20 mm away from USB, headphones, vibrators, etc.
- Layout
  1. **Do not connect crystal GND to main GND directly**. Use crystal GND trace connect to the chip's crystal GND pin, then connect it to main GND by a inner-layer short-pad below chip's crystal GND ball.
  2. **Please use AVSS18_AUXADC island as crystal reference GND due to thermal consideration.**
  3. Please make sure AUXADC two traces with well-ground shielding by GND or AVSS18_AUXADC for precise temperature measurement.
  4. Please use minimum width traces (≤ 3 mil) to do all crystal routing for thermal consideration.
  5. Isolate the XTAL1 and XTAL2 traces each other, and the length should be **4.4~10.0 mm** for thermal and signal quality consideration.
  6. Keep all crystal routing away from high-speed and power traces.
  7. Clock traces are often sensitivity and noisy, so routing these traces in inner layer is a good choice for avoiding any unwanted coupling. And, keep away from RF traces for avoiding de-sense.

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AUXADC Layout Rule

Mediatek Co-TMS Platform (PMIC)
– Crystal Layout Routing Pin Definition

PMIC	Pin Number		AUXADC Pin Number		
	XTAL1 (TMS pin1)	XTAL2 (TMS pin3)	AVDD18	VIN	AVSS18
MT6357	M1	N1	R7	T7	P7

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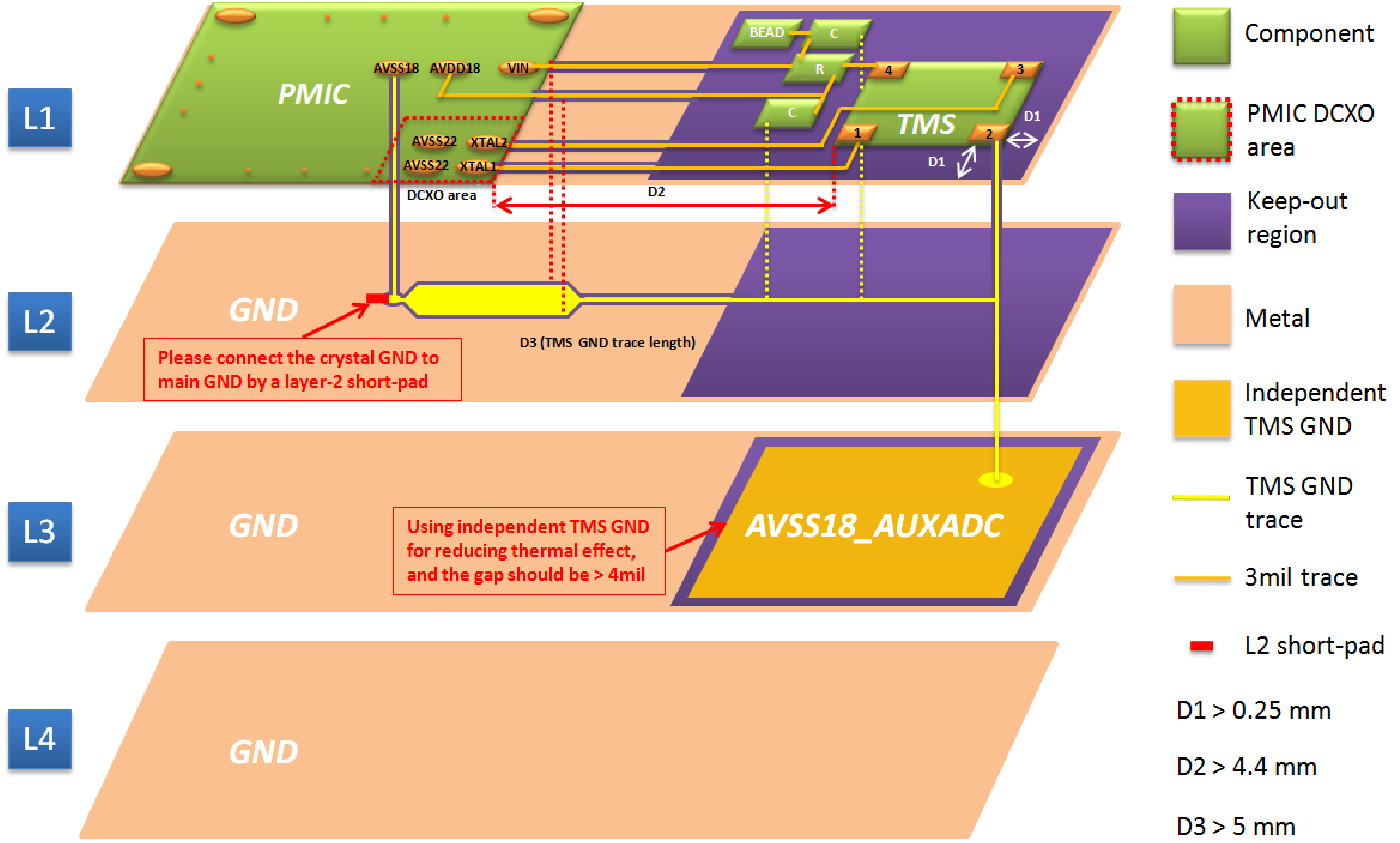
PMIC with Co-TMS Layout Recommendation

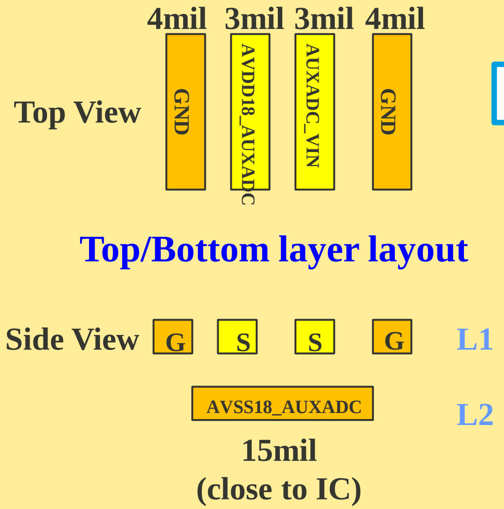
Keep the TMS and PMIC DCXO area > 10 mm away from PAs

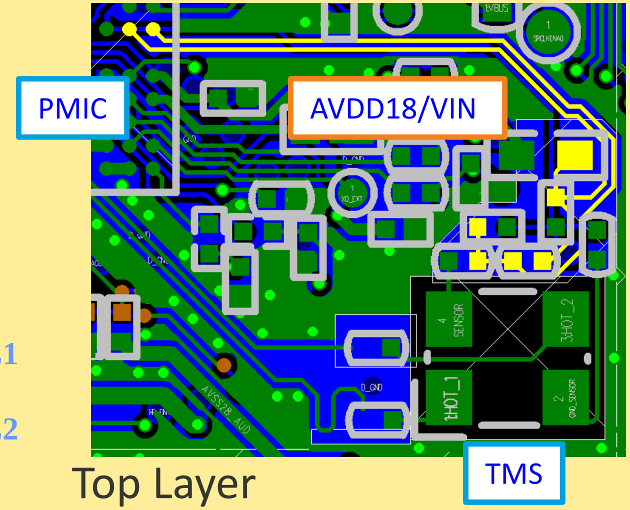


Example: AUXADC Trace Routing

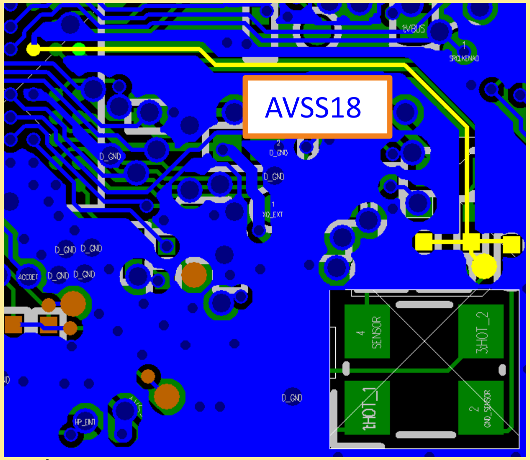
1. **(Recommended)** Routed **AVDD18/VIN** on the **top layer** and **AVSS** on the **2nd layer**.

AVDD18_AUXADC/AUXADC_VIN on the top and AUXADC_GND on 2nd layer



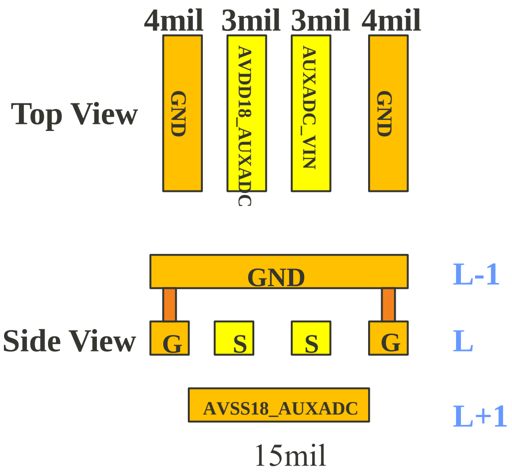


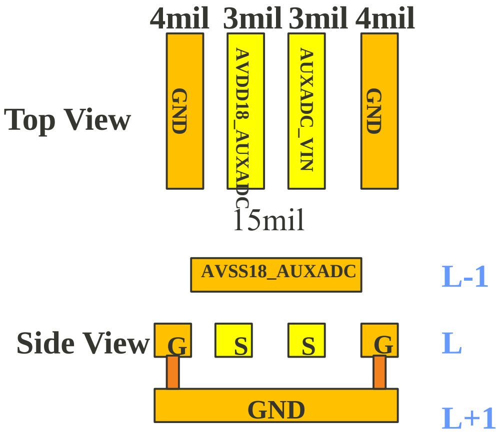
Top Layer



2nd layer

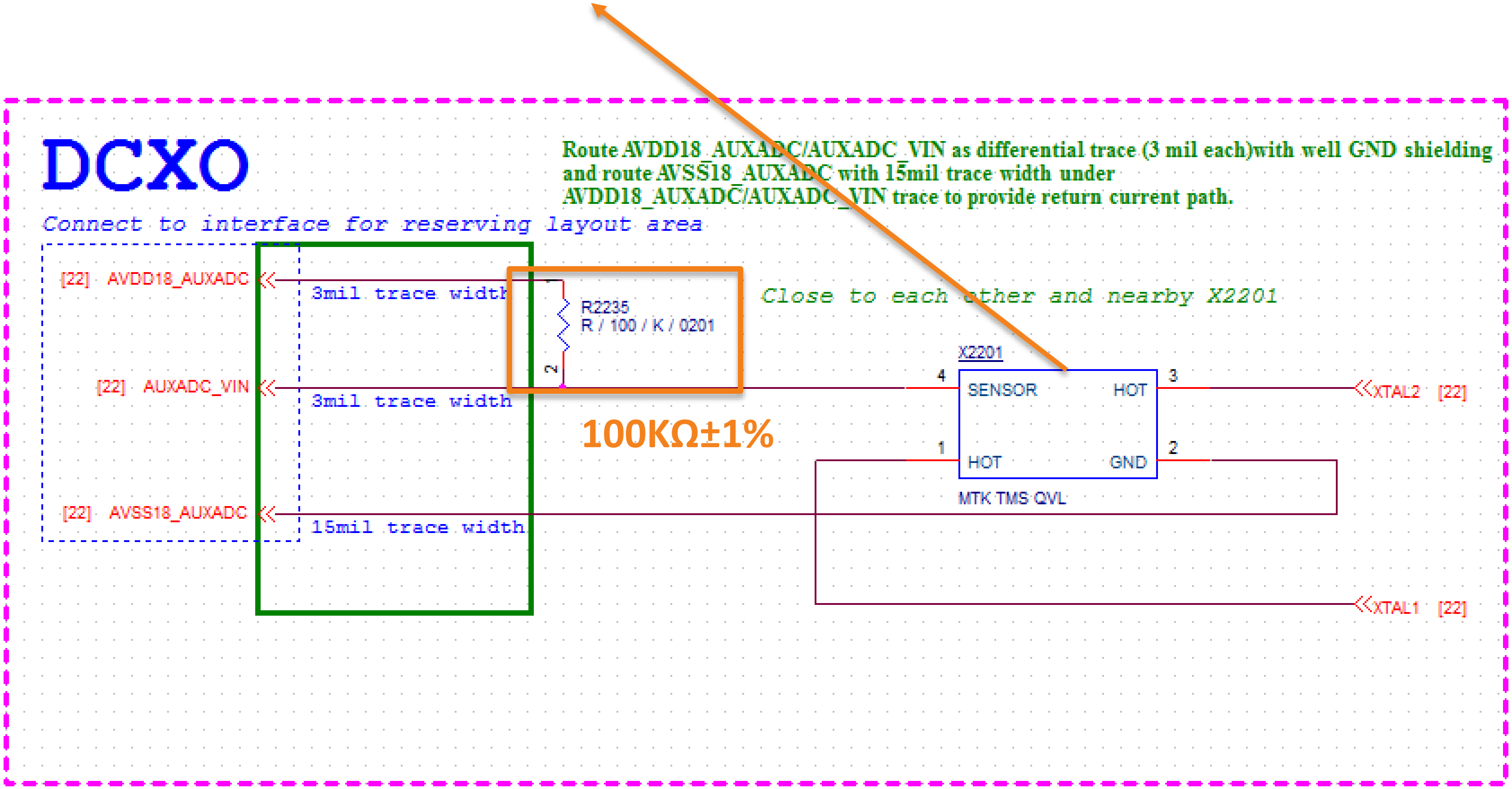
2. Routed in inner Layer is doable, but may be more difficult to follow the layout rule.



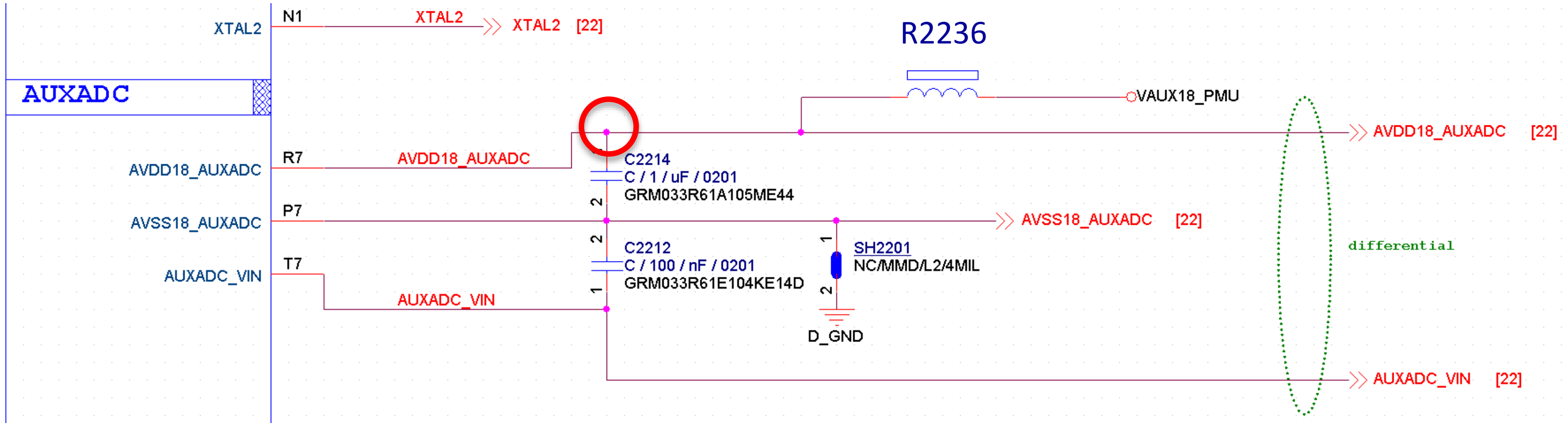


Example: GPS Co-TMS Application Circuit (1/2)

Please implement 2520 & 2016 Size TMS PCB co-layout.
Please refer to MT6765_MT6357 Co-Clock Design Notice (Page14) for co-layout guide



Example: GPS Co-TMS Application Circuit (2/2)



- Connect PMIC pin AVSS18_AUXADC to AUXADC GND first, and then connect it to main GND by a inner-layer short-pad.
- C2214 and C2212 must be closed to PMIC.
- Connect VAUX18 to C2214 first, and then connect to 100kohm and AVDD18_AUXADC.
- Follow MT6739 MTK's internal phone co-TMS layout, R2236 can use 0 ohm to replace BEAD.

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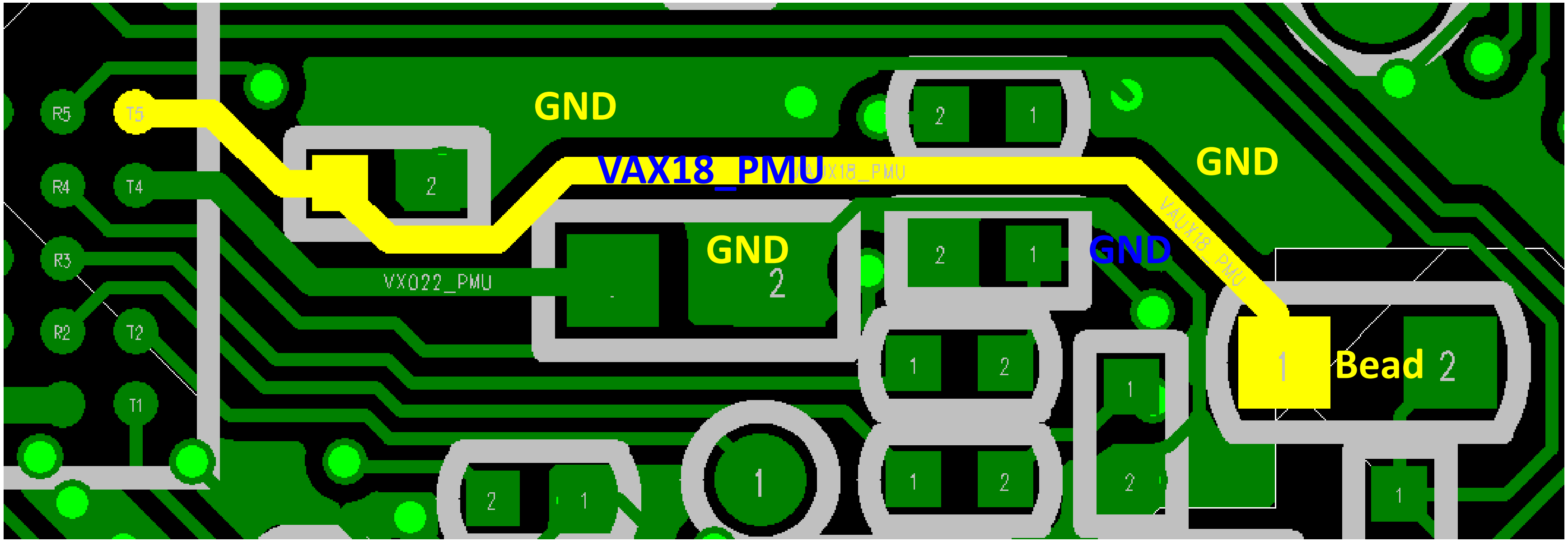
Example: VAUX18_PMU Trace Routing

- Suggest to route VAUX18_PMU on top layer with GND shielding on Top layer and Layer 2. Follow this suggestion, R2236 could use 0 ohm to replace BEAD. Please keep to use 0402 size footprint for R2236 in case need to use BEAD.



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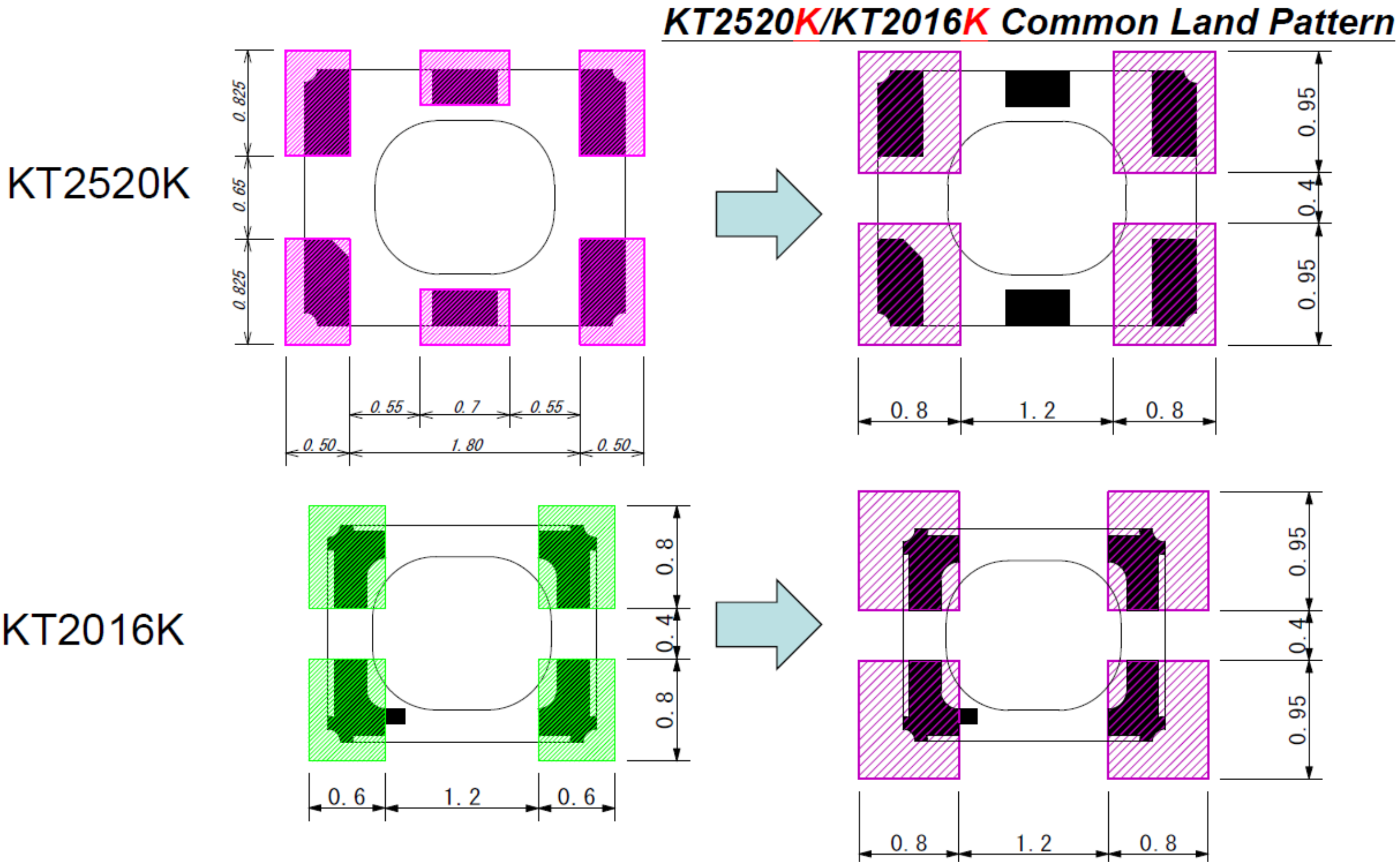
Appendix: Common Land Pattern for 2520&2016 Size TMS PCB Co-layout Suggestion



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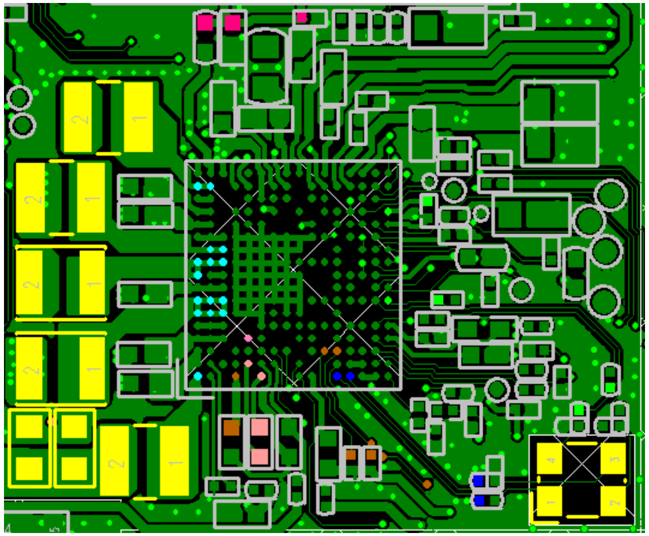
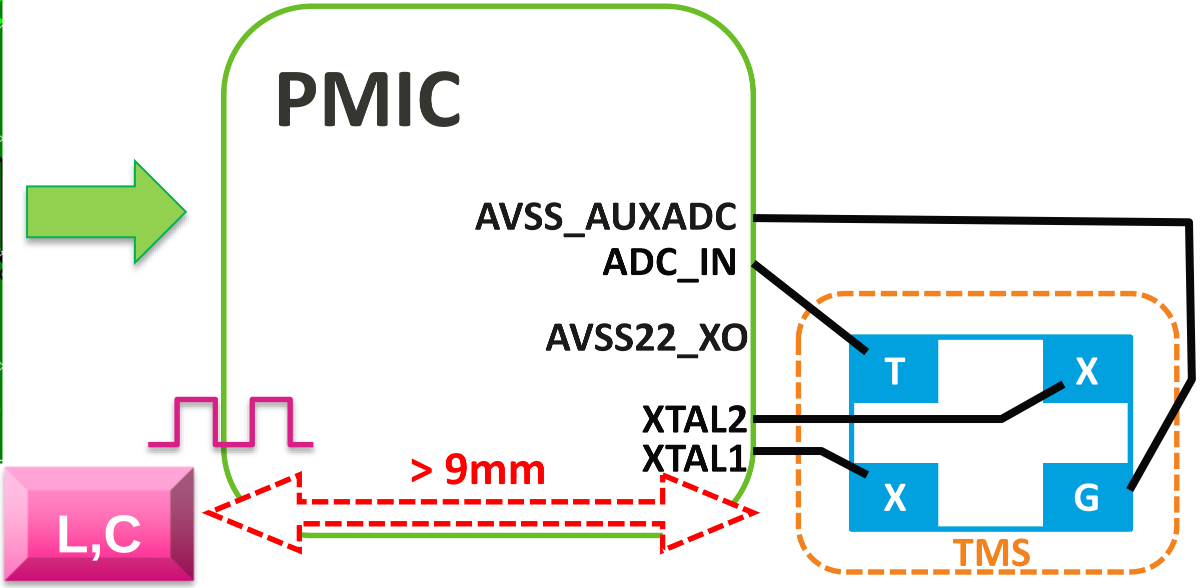
XO Layout Rule for Clock Quality

Put TMS and Input Away from Noise





XTAL1 and XTAL2 connections to TMS pin1 and pin3 can be swapped
Keep out Buck, NCP, Class-D … or other toggling signals 9mm away

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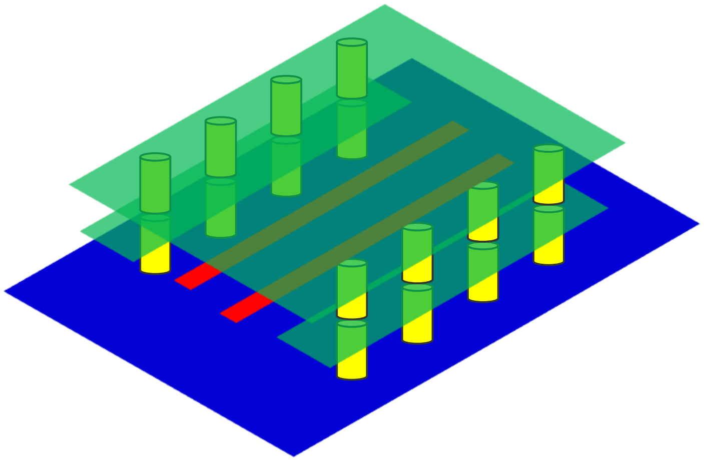
XTAL1/2 Signal Shielding Diagram

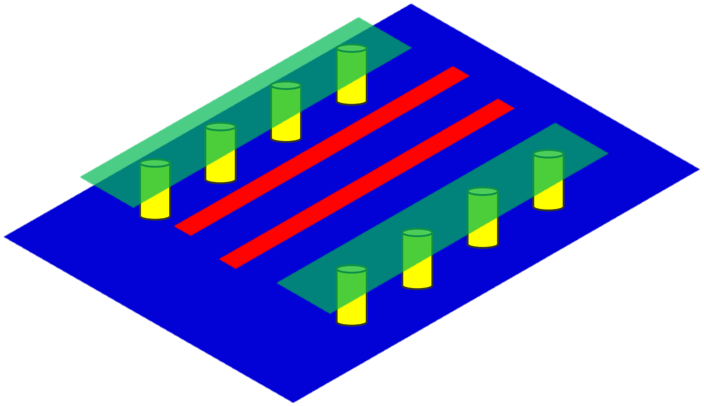
- Case 1:
  - XTAL1/2 traces are sensitivity, so routing these traces in inner layer is a good choice for avoiding any unwanted coupling.
  - Well shielding XTAL1/2 (2nd layer) with GND
  - Any other signals crossing or parallel XTAL1/2 are not allowed
- Case 2:
  - Routing XTAL1/2 on 1st layer, and with well-grounding in 1st and 2nd layers.
  - Any other signals crossing or parallel XTAL1/2 are not allowed

- XTAL1/2 signal
- Gnd
- Gnd
- via

Case 1



Case 2



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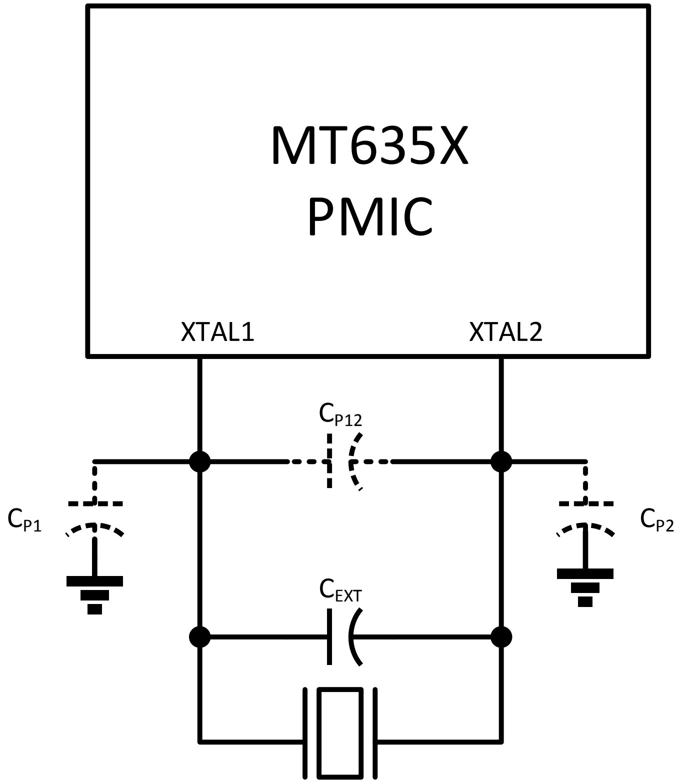
PCB board guideline for CAPID

- Add C_{EXT} for PCB tuning.
- Separate XTAL1 and XTAL2 as possible (Reduce C_{P12}).
- Total PCB capacitance
  - $C_{EQ} = C_{EXT} + C_{P12} + \frac{C_{P1}C_{P2}}{C_{P1}+C_{P2}}$



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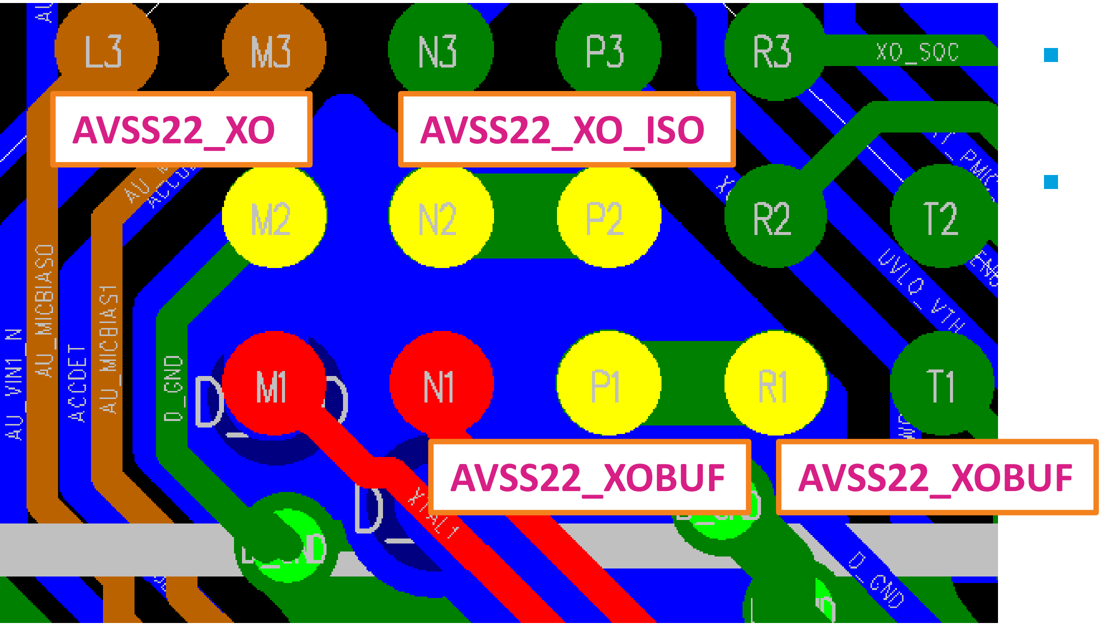
Short Them to Main GND Directly (AVSS22_XO, AVSS22_XOBUF, AVSS22_XO_ISO)



- Short them to main GND directly by the GND vias
- Shielding 26MHz buffers with AVSS22_XOBUF

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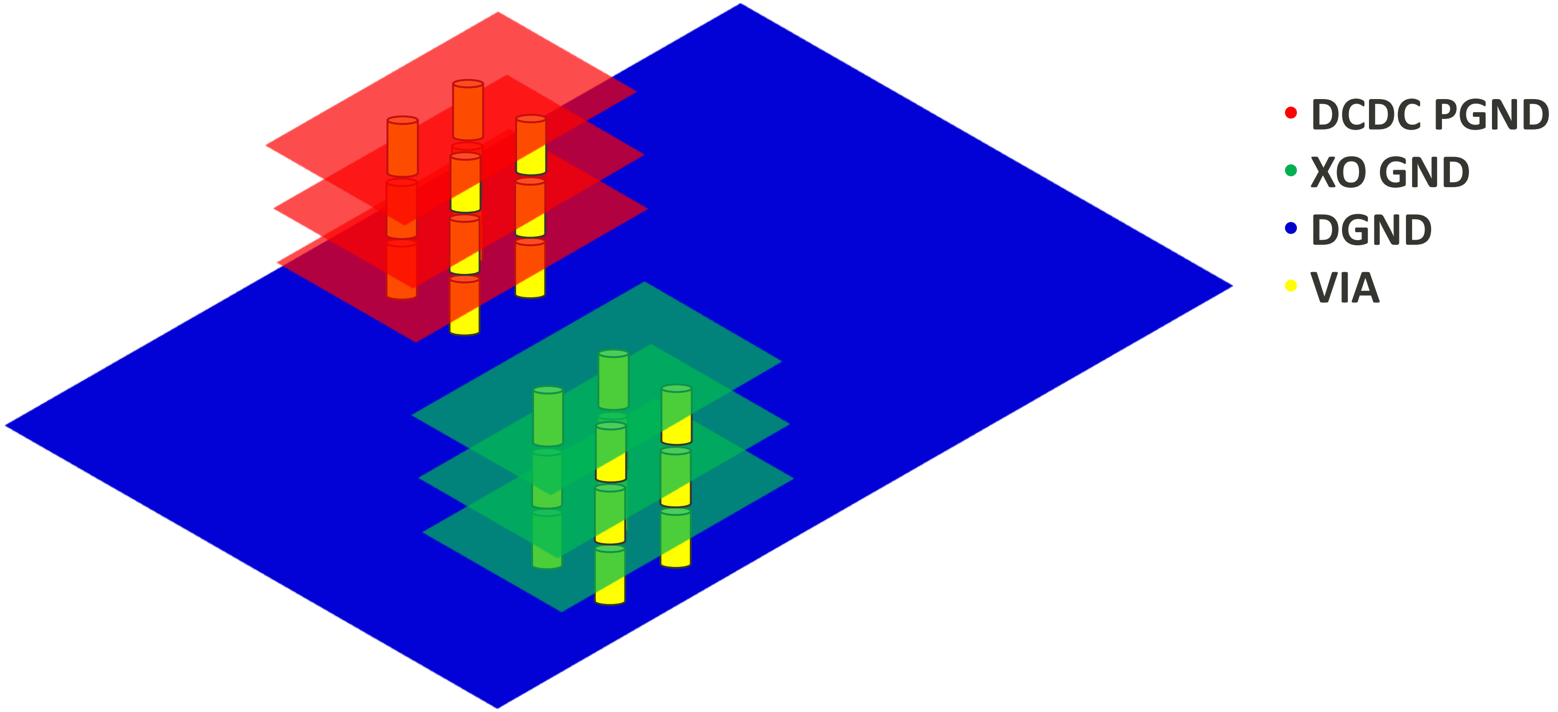
Separated Ground Islands

- Makes 2nd layer ground island for AVSS22_XO and VIAs to 4th or lower layer DGND; NOT directly connect XO GND to 2nd layer DGND
- Please DCDC PGND directly VIAs to 4th or lower DGND; NOT directly connect to TOP or 2nd layer DGND



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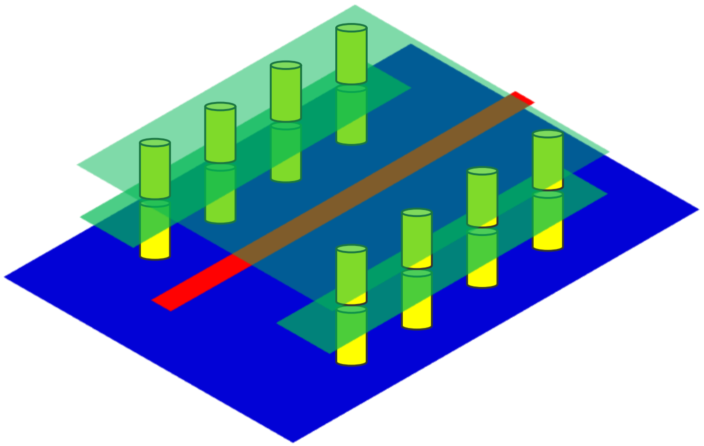
Separately ground shielding for each buffer output, XO_SOC, XO_WCN, XO_NFC, XO_CEL, XO_EXT



- ➢ **Clock traces are sensitivity and noisy, so these traces must be in inner layer or surface layer in shielding case, and not parallel with any toggling nets.**
- ➢ **Signal should be independent strip line ground shielded.**
- ➢ **Please do not parallel two signal without ground shielding**
- ➢ **Each signal routing length suggest less than 15 cm**

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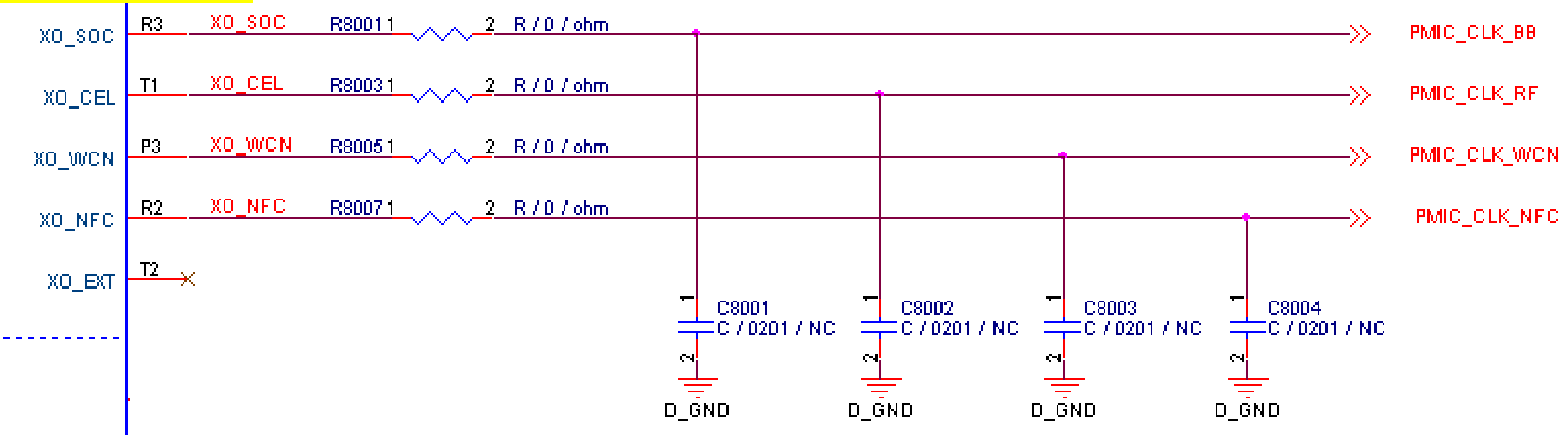
Reserved Components on Buffer Output

- **Reserve RC-network to suppress 26MHz harmonic RF de-sense risk, default keep thru signal**
- **For instance, R2214=22nH, C2209=5pF, the low pass filter corner frequency is 0.5GHz, attenuate 24dB at 2GHz**

From PMIC

To RFIC/WCN IC



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MT6357 Co-Clock Buffer setting

External Buffer Driving Controls for Harmonic Distortion

For de-sense cases, buffer driving could be changed by adjusting below CR

- **26MHz harmonic control (recommend setting)**
  - XO_SOC:
    - RG_XO_EXTBUF1_HD=2'b10 (07AE[3:2])
  - XO_WCN:
    - RG_XO_EXTBUF2_HD=2'b10 (07AE[5:4])
    - RG_XO_RESERVED4_HD[1]=1'b1 (07AA[7])
  - XO_NFC:
    - RG_XO_EXTBUF3_HD=2'b10 (07AE[7:6])
  - XO_CEL:
    - RG_XO_EXTBUF4_HD=2'b10 (07AE[9:8])
    - RG_XO_RESERVED4_HD[0]=1'b1 (07AA[6])
  - XO_EXT:
    - RG_XO_EXTBUF7_HD=2'b10 (07AE[15:14])

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Pre-driver strength for WCN/CEL slew rate

Pre-driver strength	XO_WCN register	XO_CEL register
	RG_XO_EXTBUF2_HD[1:0] RG_XO_RESERVED4_HD[1]	RG_XO_EXTBUF4_HD[1:0] RG_XO_RESERVED4_HD[0]
150ohm (min slew rate)	2'b01 1'b0	2'b01 1'b0
340ohm	2'b10 1'b0	2'b10 1'b0
800ohm (default)	2'b10 1'b1	2'b10 1'b1
1200ohm (max. slew rate)	2'b00 1'b1	2'b00 1'b1

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Pre-driver strength for SOC slew rate

RG_XO_EXTBUF1_HD	Resistor value (ohm)
00	2200 (min. slew rate)
01	1650
10	1100 (default)
11	Short (max. slew rate)

Pre-driver strength for NFC/EXT slew rate

RG_XO_EXTBUF(3/7)_HD	Resistor value (ohm)
00	800 (min. slew rate)
01	600
10	400 (default)
11	Short (max. slew rate)

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CAPID checking

- To cover the frequency tolerance and tuning sensitivity of different QVL Xtal, please make sure the calibration result of CAPID is within 60~195.
- As below example, please check the CAPID of cal. File is within 60~195.

[AFC control]
Initial value=4120
RF Chip ID=RF_ID_MT6177M
Slope=4.129032
[C2K AFC control]
AfcSlopeInv=992
CapId=174
InitDacValue=4120
[C2K BC0 RX DIV High Power]

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